A METHOD FOR IMPROVING CHIP YIELDS IN THE PRESENCE OF VIA FLARING

Abstract of the Disclosure

The current invention provides a modification procedure that reduces errors in integrated circuits due to via shorts while at the same time avoiding the unnesting of the layout design and thereby permitting verification of the layout design by LVS testing tools. The current invention identifies if potentially shorting vias have electrically redundant paths and, if so, creates cloned cells of the original cell but void of the potentially shorting vias. The cloned cell is electrically comparable to the original cell. In addition, each instantiation of the original cell in the shapes data base is replaced with the cloned cell when electrical redundancy is present. Also, the number of vias removed can be minimized or maximized while, at the same time, all via electrical shorts are removed, depending on the design requirements.

Figures